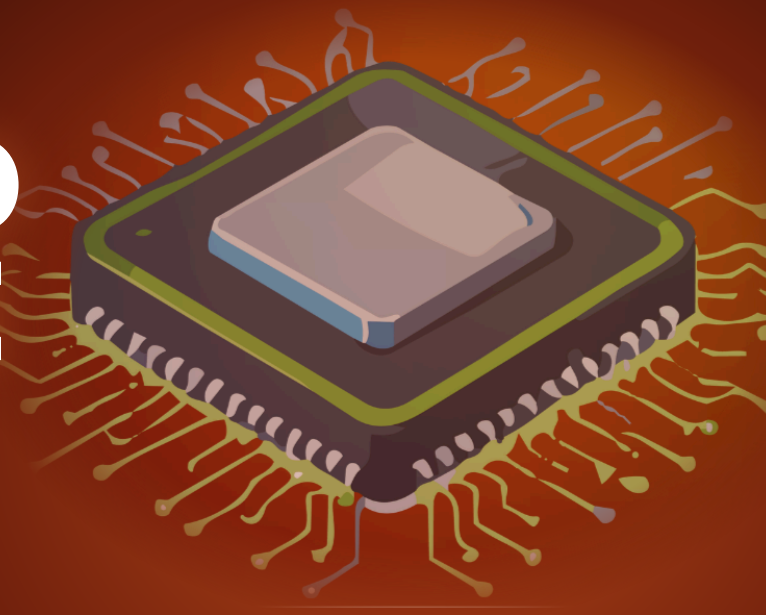
ICET 2026

Chip-DV

ICET 2026 WORKSHOP

HIGH SPEED HARDWARE

Memory Chips / ICs



A hands-on session on building and verifying high-speed memory systems and content addressable memory on FPGAs.

WHAT YOU WILL LEARN

01

High-speed memory with FPGAs

Interfacing high-speed memory chips with FPGAs: controllers, PHYs and timing.

02

CAM on FPGAs

Binary and ternary content addressable memory: architectures and trade-offs.

03

Design verification

SystemVerilog testbenches and coverage for memory subsystems.

DATE	DURATION	VENUE
Nov 18–19, 2026 During ICET 2026	3 Hours Hands-on workshop	ESIC Lab GIK Institute

LIMITED SEATS AVAILABLE

Register now

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